CLAIMS

I claim:

1. A data processing system, comprising:

a plurality of functional units;

a plurality of routing units, responsive to respective routing control signals and coupled to the plurality of functional units, by which data is steered among the plurality of functional units, the routing control signals indicating a source functional unit and a destination functional unit for a data unit; and

control word logic which supplies control words to the plurality of routing units, said control words including the routing control signals.

2. The data processing system of claim 1, wherein said plurality of routing units includes at least one multiplexer having a plurality of inputs and coupled to respective functional units in the plurality of functional units and at least one output coupled to a functional unit in the plurality of functional units, and the routing control signal for the multiplexer specifies one of a plurality of inputs to indicate a source functional unit, and one of the at least one outputs to indicate a destination functional unit.

3. The data processing system of claim 1, wherein said plurality of routing units includes at least one crossbar switch.

4. The data processing system of claim 1, wherein said plurality of functional units includes at least one storage element.

5. The data processing system of claim 1, wherein said plurality of functional units includes at least one logic block which performs a plurality of available functions, and includes logic to select an output from one of the plurality of available functions in response to a routing control signal in the control word.

6. The data processing system of claim 1, wherein said plurality of functional units includes

a memory responsive to addresses, write control signals, and read control signals, and the control word includes at least one of the write control signals and read control signals.

7. The data processing system of claim 6, wherein said control word includes an address for said memory.

8. The data processing system of claim 6, wherein an address for said memory is supplied by one of the plurality of functional units.

9. The data processing system of claim 1, wherein functional units in the plurality of functional units comprise logic dedicated to specific processing tasks.

10. The data processing system of claim 1, wherein functional units in the plurality of functional units comprise hardwired logic dedicated to specific processing tasks.

11. The data processing system of claim 1, wherein said control word logic supplies said control words synchronously to the plurality of functional units.

12. A data processing system, comprising:

a plurality of processing blocks;

a plurality of routing units, coupled to the plurality of processing blocks and responsive to respective routing control signals for the plurality of processing blocks, by which data is steered among the plurality of processing blocks; and

block level control word logic which supplies signals the plurality of routing units, said control words including the routing control signals for the processing blocks; wherein processing blocks in said plurality of processing blocks respectively include

a plurality of functional units;

a plurality of unit level routing units, coupled to the plurality of functional units and responsive to respective routing control signals for the plurality of functional units, by which data is steered among the plurality of functional units; and

functional unit level control word logic which supplies signals the plurality of routing units, said control words including the routing control signals for the plurality of functional units.

13. The data processing system of claim 12, wherein said plurality of unit level routing units includes at least one multiplexer having a plurality of inputs and coupled to respective functional units in the plurality of functional units and at least one output coupled to a functional unit in the plurality of functional units, and the routing control signal for the multiplexer specifies one of a plurality of inputs to indicate a source functional unit, and one of the at least one outputs to indicate a destination functional unit.

14. The data processing system of claim 12, wherein said plurality of block level routing units includes at least one crossbar switch.

15. The data processing system of claim 12, wherein said plurality of functional units includes at least one storage element.

16. The data processing system of claim 12, wherein said plurality of functional units includes at least one logic block which performs a plurality of available functions, and includes

logic to select an output from one of the plurality of available functions in response to a routing control signal in the control word.

17. The data processing system of claim 12, wherein said plurality of functional units includes a memory responsive to addresses, write control signals, and read control signals, and the control word includes at least one of the write control signals and read control signals.

18. The data processing system of claim 17, wherein said control word includes an address for said memory.

19. The data processing system of claim 17, wherein an address for said memory is supplied by one of the plurality of functional units.

20. The data processing system of claim 12, wherein functional units in the plurality of functional units comprise logic dedicated to specific processing tasks.

21. The data processing system of claim 12, wherein functional units in the plurality of functional units comprise hardwired logic dedicated to specific processing tasks.

22. The data processing system of claim 12, wherein at least one of said block level control word logic and functional level control word logic supplies said control words synchronously.

23. A method of processing data, in a data processing engine that includes a plurality of functional units, comprising:

providing a set of software control words that specify a route among the plurality of functional units; and

routing data among the plurality of functional units according to the set of software control words to produce a result.

24. The method of claim 21, including:

compiling a high level programming language specifying the result to produce the set of software control words.

25. The method of claim 21, wherein functional units in the plurality of functional units comprise logic dedicated to specific processing tasks.

26. The method of claim 21, wherein functional units in the plurality of functional units comprise hardwired logic dedicated to specific processing tasks.

27. The method of claim 21, wherein the data processing engine comprises a plurality of switches interconnecting the plurality of functional units, and said first and second sets of control words specify data paths through the plurality of switches.

28. The method of claim 23, including synchronously routing said data among the plurality of functional units.

29. A method of processing data, in a data processing engine that includes a plurality of functional units, comprising;

providing a first set of software control words that specify a first data path according to a first configuration of the plurality of functional units; and

providing a second set of software control words that specifies a second data path according to a second configuration of the plurality of functional units, whereby the plurality of functional units is reconfigured to perform a different function.

30. The method of claim 29, wherein functional units in the plurality of functional units comprise logic dedicated to specific processing tasks.

31. The method of claim 29, wherein functional units in the plurality of functional units comprise hardwired logic dedicated to specific processing tasks.

32. The method of claim 29, wherein the data processing engine comprises a plurality of switches interconnecting the plurality of functional units, and said first and second sets of control words specify data paths through the plurality of switches.

33. The method of claim 29, including:

compiling a high level programming language specifying the result to produce the first and second sets of software control words.